traces reflect a signal on a pin of the circuit 150, not all traces are for unique pins. For example, traces 420 and 430 may occur on the same pin. Figure 6 will be described in conjunction with the process 500 of Figure 7.

Referring now to Figure 6 and to step 510 of Figure 7, when the circuit 150 is powered on, the circuit 150 generates a lockout signal 415. This represents the period for which voltage levels are ramping up. At the end of the lockout period, a power on reset release occurs. This indicates that voltage levels are sufficient for logic operations within the circuit 150.

Referring to trace 420 of Figure 6 and step 520 of Figure 7, after the lockout period, the test controller 120 generates a synchronization pulse 425. This synchronization pulse 425 indicates that the circuit 150 is ready to negotiate entry into test mode (e.g., a ready state is entered.) The synchronization pulse 425 may appear on a single data pin of the circuit under test 150. For example, this may be a data in/out pin of the test interface 110. The length of the synchronization pulse 425 is not critical, although it may be convenient to use one half of the circuit's hold off period. This may be 8 ms, however, other periods are also suitable. Circuit 150 may use a timing reference, such as, for example, a precision oscillator (not shown) during steps of process 500. While the synchronization pulse 425 is shown as occupying the entire ready state, this is not required.

Referring to trace 430 of Figure 6 and step 530 of Figure 7, after the synchronization pulse 425, the test controller 120 monitors the test interface 110 for a digital password 435 (e.g., a password state is entered.) During this

password state, a device such as, for example, external controller 100 sends a password 435 over the test interface 110. This may be sent over the same data in/out pin as the synchronization pulse 425 was sent, although this is not required. While the digital password 435 is shown as occupying the entire password state, this is not required.

The password 435 is a bit sequence, which preferably comprises enough bits to substantially eliminate the chance of noise causing an erroneous entry into test mode. Therefore, embodiments may use any number of bits for the digital password 435.

Still referring to Figure 6, trace 440 represents a clock signal 445, which may be supplied by the external test controller 100 while it is sending the password 435. The clock signal 435 may be transmitted over the other pin of two-pin test interface 110. (E.g., clock on one pin, password on the other).

In one embodiment, the ready state and the password state take place during a circuit holdoff period, which may be, for example 16ms - 100 ms. However, the present invention is not limited to these times periods or to using the entire holdoff period or even to limiting the ready state and the password state to the chip's holdoff period. However, making use of the holdoff period, along with the lockout period 415 allows test entry negotiation to take place while the circuit 150 is otherwise under reset. Therefore, the system is not negatively impacted.

Referring now to trace 450 of Figure 6 and step 540 of Figure 7, if a valid password 435 is received within the password state, the test controller 120 sends an acknowledge signal 455 over the test interface 110.

Then, the test controller 120 enters test mode, in step 550. In test mode the test controller 120 takes control of the bus 201, while the microprocessor 210 becomes the slave.

On the other hand, if a password 445 is not detected during the password state, the circuit 150 will not enter test mode. Instead a reset exit (not shown) occurs and the circuit 150 enters normal mode of operation, in step 560.

The preferred embodiment of the present invention, a method for applying instructions to a microprocessor during test mode, is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.